University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Midterm Exam #1 – Solution
October 19, 2006

Name _____

Perm # _____

Lab Section _____

Problem #1 (20 points) _____

Problem #2 (20 points) _____

Problem #3 (20 points) _____

Problem #4 (20 points) _____

Problem #5 (20 points) _____

Total (100 points) _____

- This is a 75 minute exam; closed book, closed notes, no calculators.
- Answer all questions on the paper provided by the instructor.
- Write on only one side of the paper.
- Attach answer sheets to this exam in the correct order.
- Include your name and perm # on every sheet.

Problem #1.

1. Using only Boolean algebra, convert the following Sum of Products expression to simplified Product of Sums representation.

$$A'B + B'C'D + B'CD + A'C'D$$

$A'B + B'C'D + B'CD + A'C'D$

CONVERT TO POS ... SIMPLIFY FIRST

$A'B + B'D(C'+C) + A'C'D$

$A'B + B'D + A'C'D$

CONSENSUS TERM = $A'D$ ... $+A'C'D$

$= A'B + B'D$

TO POS: $(A'+B'D)(B+B'D)$

$(A'+B')(A'+D)(B+D)$

CONSENSUS

$(A'+B')(B+D)$

2. Again, using only Boolean algebra, convert the following Product of Sums expression to <u>simplified</u> Sum of Products representation.

$$(B' + C)(A + C' + D')(A + B')(A' + C' + D')$$

$(B'+C)(A+C'+D')(A+B')(A'+C'+D')$

$= (C'+D')$

$(B'+C)(C'+D')(A+B')$

$B'+C$

$C'+D'$

$B'C' + CC + BD' + CD'$

CONSENSUS = $B'D'$

$B'C' + CD'$

$A + B'$

$AB'C' + ACD' + B'C' + B'CD'$

ABSORPTION

$ACD' + B'C' + B'CD'$

$ACD' + B'(C' + CD')$

$ACD' + B'(C' + D')$

$= ACD' + B'C' + B'D'$

3. Again (and finally), using only Boolean algebra, prove the following theorem:

$$(X+Y)(X'+Z)(Y+Z) = (X+Y)(X'+Z)$$

$(x+y)(x'+z)(y+z) = (x+y)(x'+z)$

$(x+y)(x'+z)(y+z+xx')$

$(x+y)(x'+z)(y+z+x)(y+z+x')$

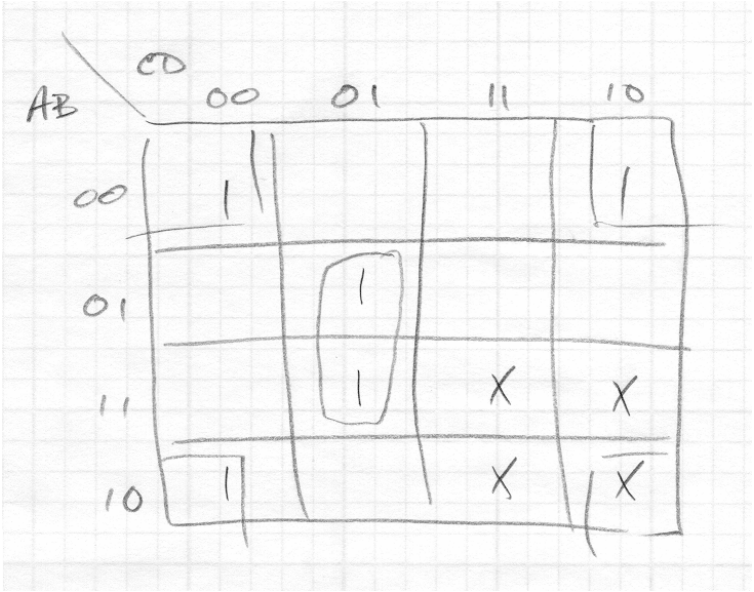
By ABSORPTION

$(x+y)(x'+z)$

Problem #2.

1. Map the following sum of minterms function on a Karnaugh map:

$$\Sigma m = (0,2,5,8,13) + d(10,11,14,15)$$



2. Identify all prime and essential prime implicants and minimize the function.

PRIME IMPLICANTS

$B'D'$, $BC'D$

BOTH ARE ESSENTIAL

3. Is the minimized sum of products expression unique (and why or why not)?

UNIQUE BECAUSE COVER INCLUDES ONLY ESSENTIAL PRIME IMPLICANTS

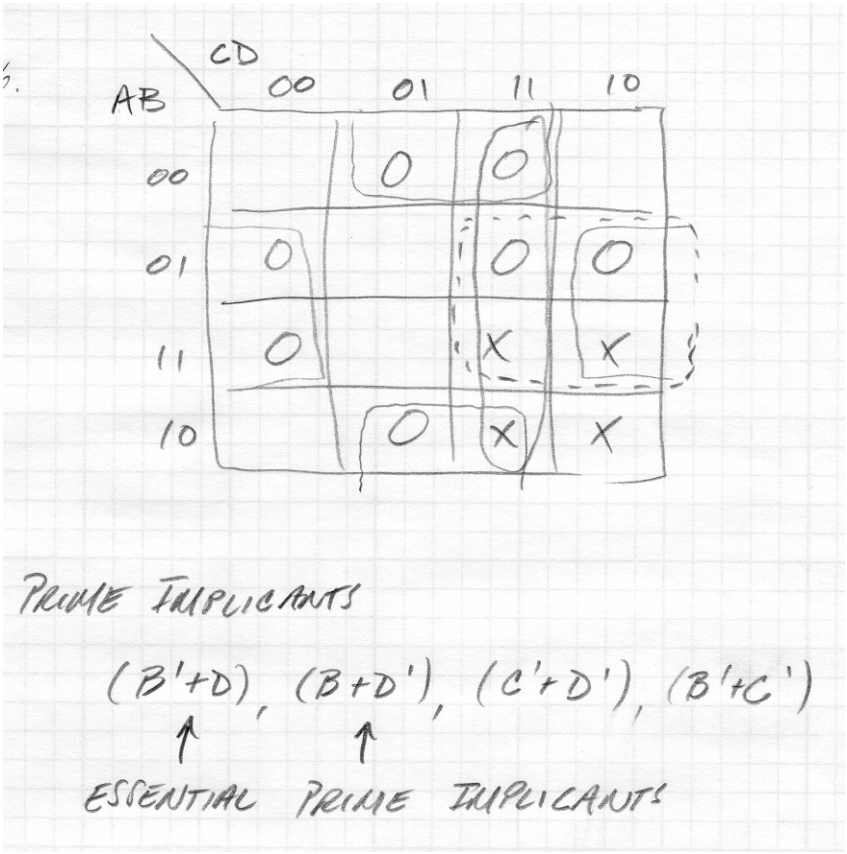
4. As implemented in part 2 above, express the minimized function in sum of minterms form.

$\Sigma_m(0, 2, 5, 8, 10, 13)$

5. Express the same function from part 1 above, in product of maxterms form.

$\Pi_M(1, 3, 4, 6, 7, 9, 12) \cdot d(10, 11, 14, 15)$

6. Map the product of maxterms function, identify all prime and essential prime implicants and minimize the function.



7. Is the minimized product of sums expression unique (and why or why not)?

NOT UNIQUE

$= (B'+D)(B+D')(C'+D')$

OR

$= (B'+D)(B+D')(B'+C')$

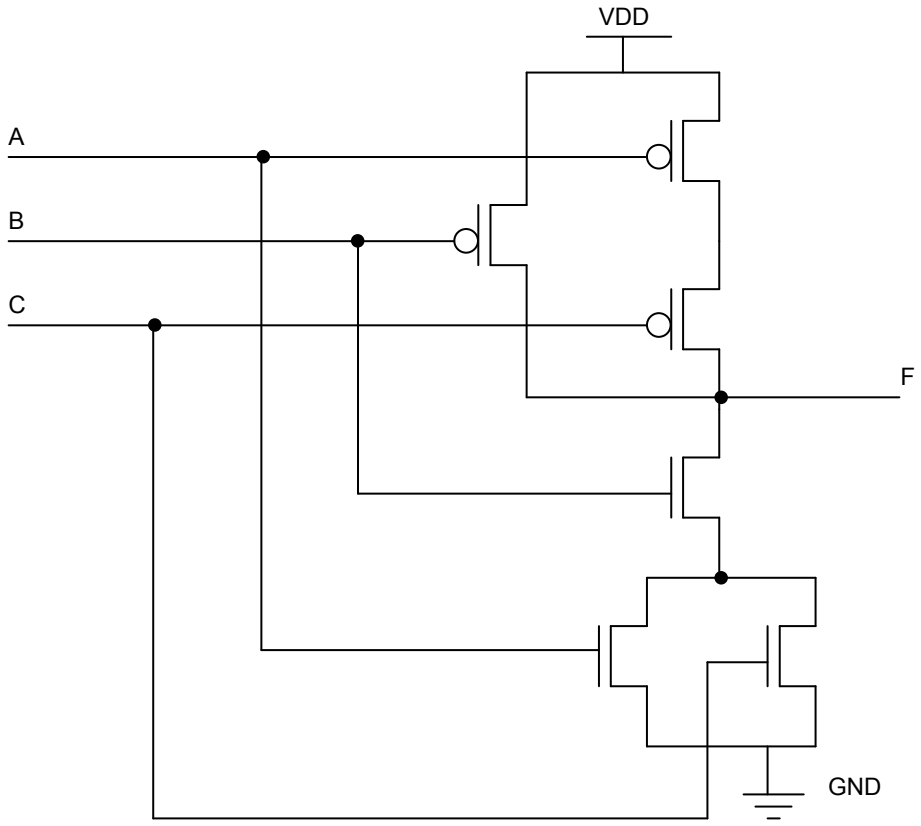
8. As implemented in part 6 above, express the minimized function in product of maxterms form.

$\Pi M = (1, 3, 4, 6, 7, 9, 11, 12, 14, 15)$

Problem #3.

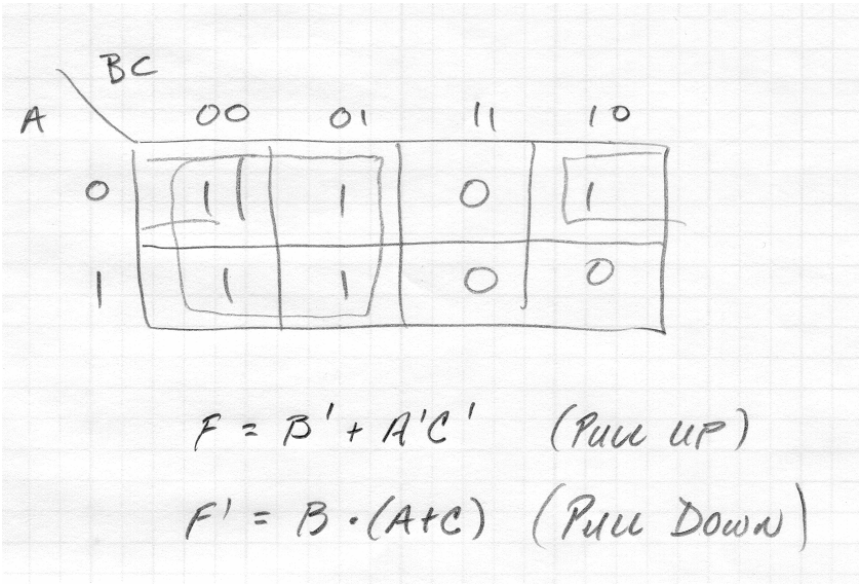
The static CMOS gate shown below is knows as a “complex gate” because it includes both parallel and serial paths in both the pull-up network (pMOS transistors to logic “1”) and the pull-down network (nMOS transistors to logic “0”).

1. Construct the truth table for the compound gate shown below.



A	B	C	F	
0	0	0	1	} B = 0 PMOS ON
0	0	1	1	
0	1	0	1	← A = C = 0 PMOS ON
0	1	1	0	← B = C = 1 nMOS ON
1	0	0	1	} B = 0 PMOS ON
1	0	1	1	
1	1	0	0	← B = A = 1 nMOS ON
1	1	1	0	← A = B = C = 1 nMOS ON

2. What function is implemented (Boolean expression) by this gate?

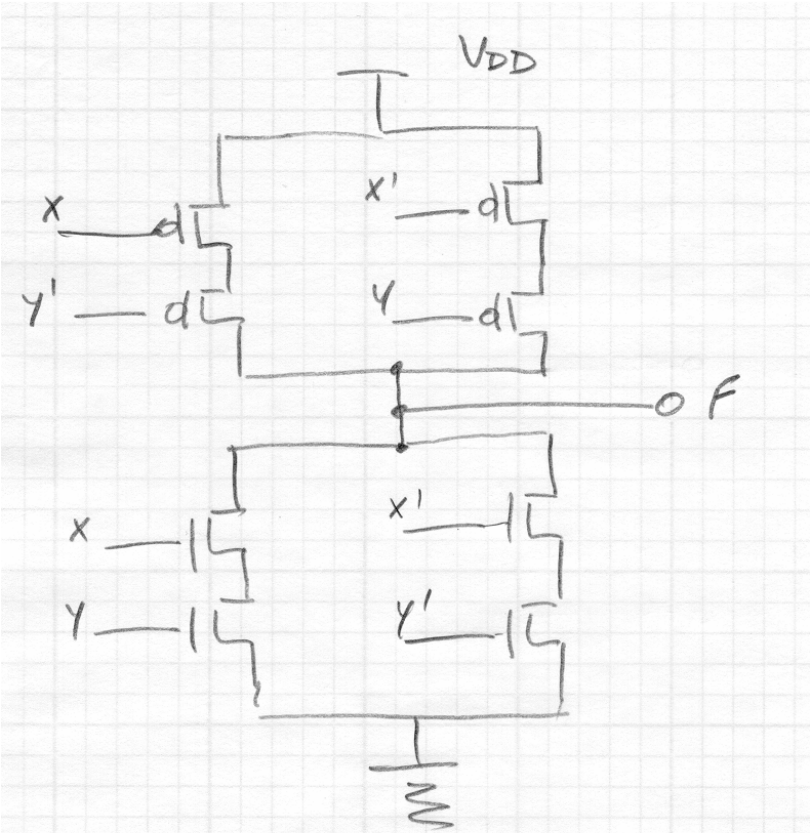


$F = B' + A'C'$ (Pull up)

$F' = B \cdot (A+C)$ (Pull Down)

3. The sum output of a half adder (XOR) can be constructed from a single, complex gate, assuming both the true and complemented versions of both inputs, x and y, are available (i.e., x, x', y and y').

   Design the complex CMOS gate that implements the sum output of a half adder. As always, use pMOS transistors to pass "1's" to the output and nMOS transistors to pass "0's".



$F = XY' + X'Y$ (Pull Up)

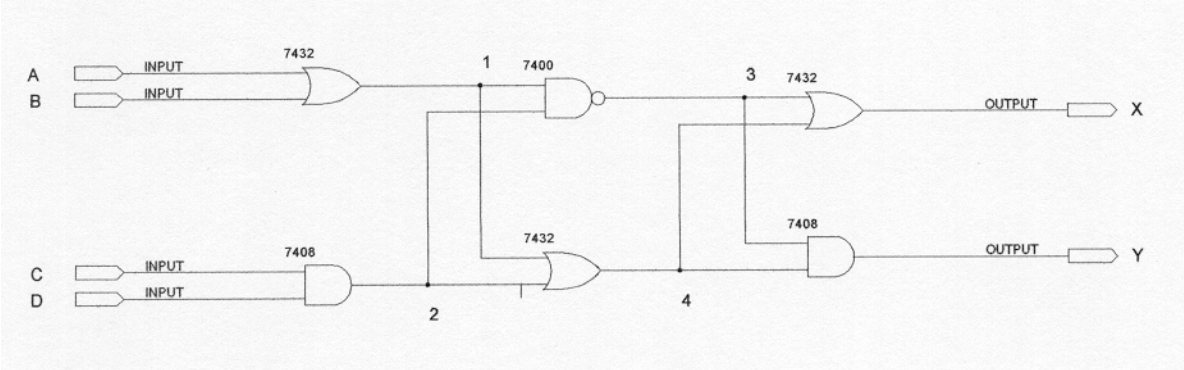
$F' = (X'+Y)(X+Y')$

$XY + X'Y'$ (Pull Down)

Problem #4.

For the network shown below, determine the critical path and maximum propagation delay. The NAND, AND and OR gates have the following propagation delays:

		t_{PLH}	t_{PHL}
7400	NAND	22ns	15ns
7408	AND	27ns	19ns
7432	OR	15ns	22ns



1. Define the path from input to output and identify the nodes (indicated 1, 2, 3 and 4 on the schematic) constituting the critical path. Be sure to take inversions into account when determining the maximum propagation delay.

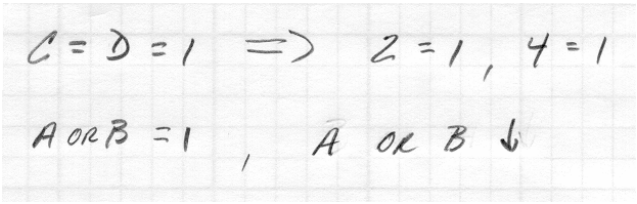
A (OR B) → 1 → 3 → Y

2. What is the maximum propagation delay and how is it determined (which propagation delays are used in the calculation)?

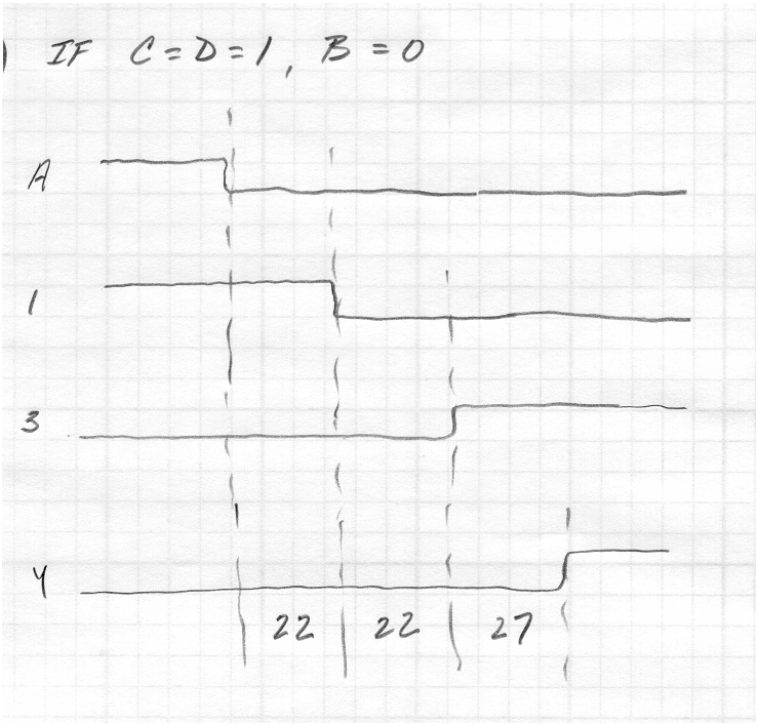
7432 t_{PHL} + 7400 t_{PLH} + 7408 t_{PLH}

22 + 22 + 27 = 71nS

3. What must the other inputs be in order to allow the signal to propagate from the input to the output?



4. Construct a timing diagram illustrating the delays along the critical path (showing all relevant internal nodes) and including both the X and Y outputs.



Other paths within 5% of 71ns path:

1) C (OR D) → 2 → 4 → Y

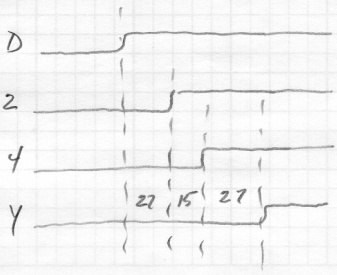
2) 7408 t_{PLH} + 7432 t_{PLH} + 7408 t_{PLH}

27 + 15 + 27 = 69nS

3) A = B = 0 ⇒ 1 = 0, 3 = 1

C OR D = 1, D OR C ↑

4) A = B = 0, C = 1



1) C (OR D) → 2 → 3 → Y

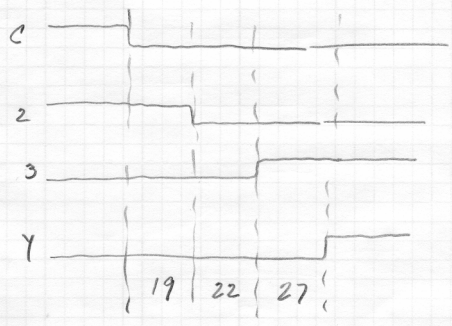
2) 7408 t_{PHL} + 7400 t_{PLH} + 7408 t_{PLH}

19 + 22 + 27 = 68nS

3) A = B = 1 ⇒ 1 = 1, 4 = 1

C AND D = 1, C OR D ↓

4) IF A = B = C = D = 1



Problem #5.
In this problem you are to design a portion of the circuitry that locks the doors and opens the windows of my car.

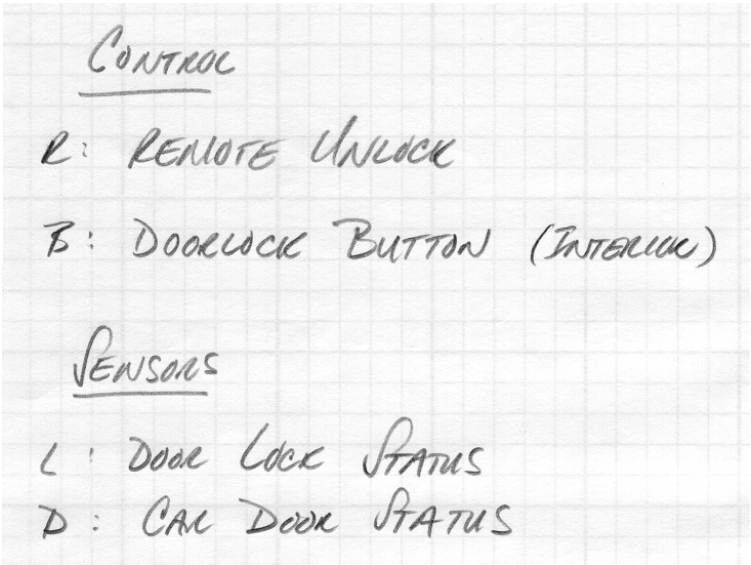
There are four inputs to the circuit: the remote unlock button (R) on my key, the door lock button (B) on the console inside the car, an input indicating the status of the door locks (L : 1 when locked, 0 when unlocked) and an input indicating whether the car doors are open or closed (D : 1 when all are closed, 0 when any are open).

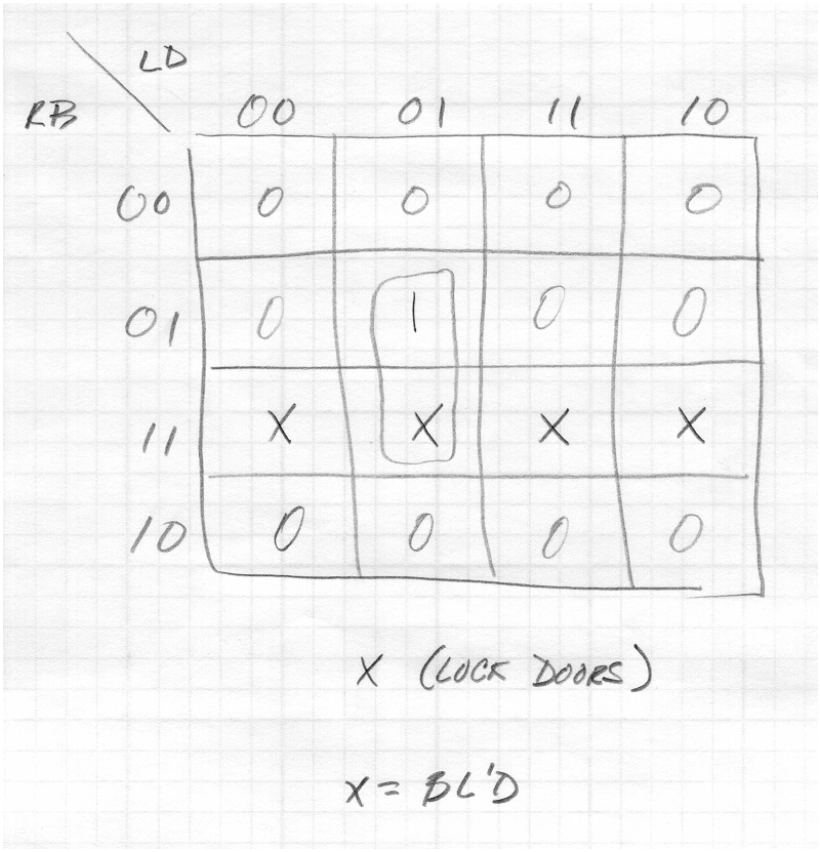
The circuit has three outputs: lock doors (X), unlock doors (U) and open windows (W).

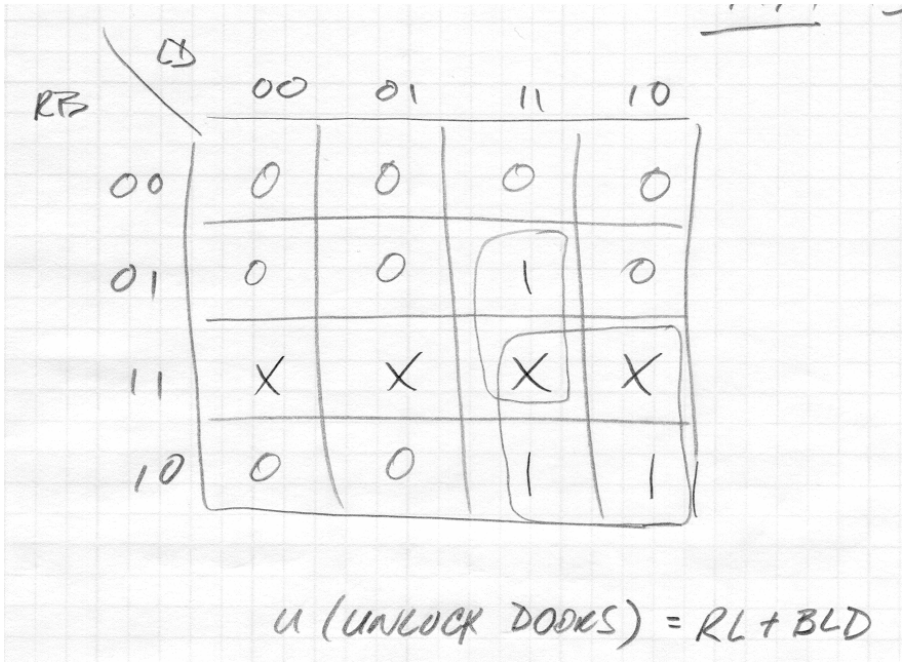
The interior door lock button only works when all of the doors are closed. When pressed with the doors locked, the doors are unlocked. When pressed with the doors unlocked, the doors are locked.

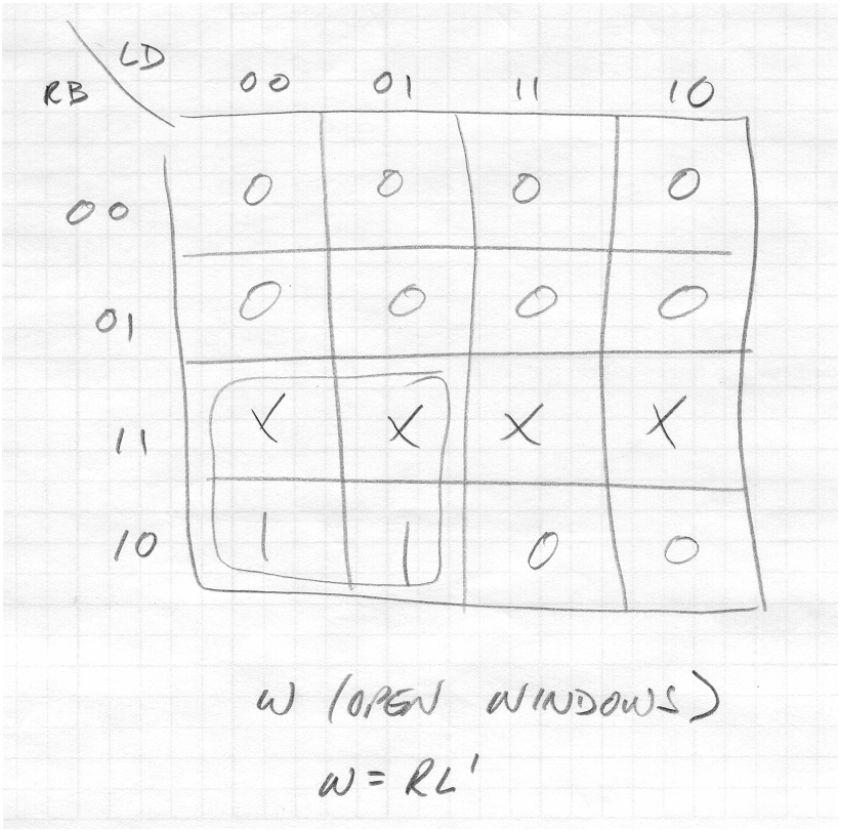
The remote unlock button unlocks the doors when the doors are locked and opens the windows when the doors are unlocked. The remote unlock button does not work inside the car and works whether the doors are open or closed.

1. Design the 4-input, 3-output circuit that implements this door entry system. Specify your design in sum of products form and clearly identify any assumptions. You don't have to draw the circuit; the simplified Boolean function is adequate.




LD
RB
00 01 11 10
00 0 0 0 0
01 0 1 0 0
11 X X X X
10 0 0 0 0
X (LOCK DOORS)
X = BL'D


LD
RB
00 01 11 10
00 0 0 0 0
01 0 0 1 0
11 X X X X
10 0 0 1 1
U (UNLOCK DOORS) = RL + BLD



There is also a remote lock button ("RL") on my key. When the doors are unlocked and the remote lock button is pressed, the doors are locked. If the doors are already locked, the interior lights ("IL") are illuminated. Like the remote unlock button, it does not work inside the car and it's ergonomically impossible to press the remote lock and remote unlock buttons at the same time.

2. Add the remote lock input and the interior light output to the circuit designed above. Again, as above, specify your design in sum of products form and clearly identify any assumptions. You don't have to draw the circuit; the simplified Boolean function is adequate.

REMOTE LOCK BUTTON

- AFFECTS X (LOCK DOORS) AND IL (INTERIOR LIGHTS)
- PREVIOUSLY X = BL'D
  - L DOORS CLOSED
  - D DOORS UNLOCKED
  - B INTERIOR BUTTON

- NOW:

RB \ LD	00	01	11	10
00	1	1	0	0
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

RL = 1 X (LOCK DOORS)

- WITH $RL = 0$

$$X = BL\bar{D} \quad \text{(AS BEFORE)}$$

- WITH $RL = 1$

$$X = RL \cdot L' \Rightarrow X = BL\bar{D} + RL \cdot L'$$

BY INSPECTION,

$$IL = RL \cdot L$$